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-- Company:

-- Engineer:

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-- Create Date: 18:13:10 01/28/2020

-- Design Name:

-- Module Name: U:/EECE359 Labs/Lab1/Test\_UART.vhd

-- Project Name: Lab1

-- Target Device:

-- Tool versions:

-- Description:

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-- VHDL Test Bench Created by ISE for module: UART

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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-- Notes:

-- This testbench has been automatically generated using types std\_logic and

-- std\_logic\_vector for the ports of the unit under test. Xilinx recommends

-- that these types always be used for the top-level I/O of a design in order

-- to guarantee that the testbench will bind correctly to the post-implementation

-- simulation model.

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LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--USE ieee.numeric\_std.ALL;

ENTITY Test\_UART IS

END Test\_UART;

ARCHITECTURE behavior OF Test\_UART IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT UART

PORT(

TXD : OUT std\_logic;

RXD : IN std\_logic;

CLK : IN std\_logic;

DBIN : IN std\_logic\_vector(7 downto 0);

DBOUT : OUT std\_logic\_vector(7 downto 0);

RDA : OUT std\_logic;

TBE : OUT std\_logic;

RD : IN std\_logic;

WR : IN std\_logic;

PE : OUT std\_logic;

FE : OUT std\_logic;

OE : OUT std\_logic;

RST : IN std\_logic

);

END COMPONENT;

--Inputs

signal RXD : std\_logic := '0';

signal CLK : std\_logic := '0';

signal DBIN : std\_logic\_vector(7 downto 0) := (others => '0');

signal RD : std\_logic := '0';

signal WR : std\_logic := '0';

signal RST : std\_logic := '0';

--Outputs

signal TXD : std\_logic;

signal DBOUT : std\_logic\_vector(7 downto 0);

signal RDA : std\_logic;

signal TBE : std\_logic;

signal PE : std\_logic;

signal FE : std\_logic;

signal OE : std\_logic;

-- Clock period definitions

constant CLK\_period : time := 31.25 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: UART PORT MAP (

TXD => TXD,

RXD => RXD,

CLK => CLK,

DBIN => DBIN,

DBOUT => DBOUT,

RDA => RDA,

TBE => TBE,

RD => RD,

WR => WR,

PE => PE,

FE => FE,

OE => OE,

RST => RST

);

-- Clock process definitions

CLK\_process :process

begin

CLK <= '0';

wait for CLK\_period/2;

CLK <= '1';

wait for CLK\_period/2;

end process;

-- Stimulus process

stim\_proc: process

procedure transmit\_data(data: in std\_logic\_vector (7 downto 0)) is

begin

while TBE = '0' loop

wait for CLK\_period;

end loop;

DBIN <= data;

wait for CLK\_period;

WR <= '1';

wait for 40 us;

WR <= '0';

report "TEST BENCH WROTE DATA TO DBIN";

end procedure;

begin

RXD <= '1';

RST <= '1';

-- hold reset state for 100 ns.

wait for 15 us;

RST <= '0';

wait for CLK\_period\*10;

transmit\_data("10101010");

transmit\_data("01010101");

transmit\_data("01100111");

wait;

end process;

END;